Claims

1. A method for forming a body region in a drain region of a DMOS device on a wafer after the gate has been formed with the body region extending partly beneath a gate of the DMOS device and appropriately aligned with the gate, the drain region defining a surface plane, the method comprising the steps of:

(a) implanting a suitable dopant in a portion of the drain region adjacent the gate for forming the body region to have a desired drain/source threshold voltage, and

(b) implanting a suitable dopant in the said portion of the drain region adjacent the gate for forming the body region to have a desired breakdown voltage through the drain region,

steps (a) and (b) being performed in any order, and the dopant being implanted in step (a) by directing the dopant at a first angle to the surface plane of the drain region for directing at least some of the dopant beneath the gate, the first angle to the surface plane at which the dopant is directed in step (a) being less than a second angle to the surface plane at which the dopant is directed in step (b).

2. A method as claimed in Claim 1 in which the dopant is directed at the first angle towards the surface plane in step (a) in a general source/drain direction.

3. A method as claimed in Claim 1 in which the dopant is directed at the second angle towards the surface plane in step (b) in a general source/drain direction.

4. A method as claimed in Claim 1 in which the first angle to the surface plane of the drain region at which the dopant is directed in step (a) lies in the range of 30° to 60°.

5. A method as claimed in Claim 4 in which the first angle to the surface plane of the drain region at which the dopant is directed in step (a) is approximately 45°.

6. A method as claimed in Claim 1 in which the second angle to the surface plane of the drain region at which the dopant is directed in step (b) lies in the range of 70° to 90°.

7. A method as claimed in Claim 6 in which the second angle to the surface plane of the drain region at which the dopant is directed in step (b) is approximately 83°.

8. A method as claimed in Claim 1 in which the dopant is implanted in the drain region in each of steps (a) and (b) using an edge of the gate adjacent the source as part of a mask for defining a portion of the surface of the drain region through which the dopant is to be implanted.

9. A method as claimed in Claim 1 in which the dopant implanted in each of steps (a) and (b) may be the same or different, and the dopant implanted in each of steps (a) and (b) may be implanted at the same or different dose and/or energy levels.

10. A method as claimed in Claim 1 in which the dopant implanted in the drain region in each of steps (a) and (b) is diffused by a dopant diffusion process for forming the body region.

11. A method as claimed in Claim 1 in which the drain region is formed by an N-well, and the body region is formed as a P-body, and the dopant of each of steps (a) and (b) is boron.

12. A method as claimed in Claim 1 in which the drain region is formed by a P-well, and the body region is an N-body, and the dopant of each of steps (a) and (b) is phosphorous.

13. A method as claimed in Claim 1 in which the dose and energy levels of the dopant implanted in each of steps (a) and (b) are sufficient for providing the desired drain/source threshold voltage and the breakdown voltage through the drain region.

14. A method as claimed in Claim 1 in which the method for forming the body region in the drain region of the DMOS device is a CMOS process.

15. A method as claimed in Claim 1 in which the DMOS device is an LDMOS device.

16. A DMOS device comprising a drain region defining a surface plane, a gate located on the drain region, and a body region formed in the drain region and

extending partly beneath the gate and appropriately aligned therewith, the body region being formed after the gate region has been formed by:

(a) implanting a suitable dopant in a portion of the drain region adjacent the gate for forming the body region to have a desired drain/source threshold voltage, and

(b) implanting a suitable dopant in the said portion of the drain region adjacent the gate for forming the body region to have a desired breakdown voltage through the drain region,

steps (a) and (b) being performed in any order, and the dopant being implanted in step (a) by directing the dopant at a first angle to the surface plane of the drain region for directing at least some of the dopant beneath the gate, the first angle to the surface plane at which the dopant is directed in step (a) being less than a second angle to the surface plane at which the dopant is directed in step (b).

17. A DMOS device as claimed in Claim 16 in which the dopant is directed at the first angle towards the surface plane in step (a) in a general source/drain direction.

18. A DMOS device as claimed in Claim 16 in which the dopant is directed at the second angle towards the surface plane in step (b) in a general source/drain direction.

19. A DMOS device as claimed in Claim 16 in which the first angle to the surface plane of the drain region at which the dopant is directed in step (a) lies in the range of 30° to 60°.

20. A DMOS device as claimed in Claim 19 in which the first angle to the surface plane of the drain region at which the dopant is directed in step (a) is approximately 45°.

21. A DMOS device as claimed in Claim 16 in which the second angle to the surface plane of the drain region at which the dopant is directed in step (b) lies in the range of 70° to 90°.

22. A DMOS device as claimed in Claim 21 in which the second angle to the surface plane of the drain region at which the dopant is directed in step (b) is approximately 83°.

23. A DMOS device as claimed in Claim 16 in which the body region in the drain region of the DMOS device is formed by a CMOS process.

24. A DMOS device as claimed in Claim 16 in which the DMOS device is an LDNMOS device.

25. A DMOS device as claimed in Claim 16 in which the DMOS device is and LDPMOS device.

26. An integrated circuit chip comprising a DMOS device as claimed in Claim 16.

27. An integrated circuit chip comprising a DMOS device formed thereon by the method of Claim 1.